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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/725,704	11/29/2000	Thomas J. Cloonan	4807.00017	8828

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ARRIS INTERNATIONAL, INC
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EXAMINER	
LAMBRECHT, CHRISTOPHER M	
ART UNIT	**PAPER NUMBER**
2623	

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/725,704	CLOONAN ET AL.	
	Examiner	Art Unit	
	Christopher M. Lambrecht	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

2. Claims 11, 15, 20, and 24 are objected to because of the following informalities: Claim 11 at line 11, replace "master" with --first--. The same objection applies to claim 15 at line 9, claim 20 at line 10, and claim 24 at line 9. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salee, U.S. Patent Application Publication No. 2002/0088003, in view of Lovett et al. (Lovett), U.S. Patent No. 6,591,370, in view of Eatherton, U.S. Patent No. 6,697,382.

Regarding claims 11, 15, 20, and 24, Salee discloses a cable modem termination system (CMTS) with a plurality of cable interface circuits (10, 20) each of which includes a cyclical timing counter (24) that provides timing signals to cable modems (CMs) coupled to each of said interface circuits (¶¶ 12-13). Salee further discloses a

system controller means (10) for and method of synchronizing the timing counters (24) of a first cable interface circuit (10) and a second cable interface circuit (20) comprising the steps of: copying a first value (P) of said timing counter (24) of said first cable interface circuit (10) into a storage device (26) (¶ 14); copying said first timing counter value (P) into a storage device (26) that is local with respect to the second cable interface circuit (20) (¶ 14); and copying the value from said storage device (26) that is local with respect to the second cable interface circuit (20) into said timing counter (24) of said second cable interface circuit (20) (¶ 14).

Salee fails to disclose adding an offset to the first timing value, such that the value copied into the storage device local to the second cable interface card is a future timing counter value, i.e., the sum of the first timing counter value and the offset, wherein the offset amount includes the time to transfer a timing value from the first timing counter into a storage device local to the second cable interface circuit.

In an analogous art, Lovett discloses a method for synchronizing the timing counters of a first circuit (13) and second circuit (12) (col. 3, l. 65 - col. 4, l. 7). The method includes copying a first timing counter value of the first circuit (source node) into a storage device (108) (col. 6, ll. 1-7); copying said first timing counter value into a storage device (82) that is local with respect to the second circuit (node being synchronized) (col. 6, ll. 16-18); adding an offset (elapsed time) to said first timing counter value to create a future timing counter value, the future timing counter value being the sum of said first timing counter value and the offset (col. 6, ll. 22-27), wherein

the offset amount includes the time to transfer the first timing counter value from the first timing counter into the storage device local to the second circuit (col. 6, ll. 20-22); and copying said future timing counter value into the timing counter (86) of said second circuit (col. 6, ll. 27-30). Lovett further discloses that the disclosed method enables circuits to be added to the system without effecting the synchronization of the other circuits in the system (col. 6, ll. 33-39), thereby preventing disruption of current packet-based communications sessions executing on system nodes (col. 1, ll. 48-62).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Salee to include adding an offset to the first timing value copied into the storage device local to the second cable interface card to create a future timing counter value that is the sum of the first timing counter value and the offset, wherein the offset amount includes the time to transfer a timing value from the first timing counter into a storage device local to the second cable interface circuit, for the benefit of enabling new cable interface circuits to be added and synchronized to the first cable interface circuit without disrupting current communication sessions executing on active cable interface circuits.

Salee in view of Lovett fails to disclose that the offset is added to the first timing counter value before said first timing counter value is copied to the storage device local to the second cable interface circuit.

In an analogous art, Eatherton discloses a method of synchronizing timing counters of first and second interface circuits (169, 179) in a packet switching system

(col. 3, ll. 40-57). Similar to Lovett, Eatherton discloses adding an offset (delay) to a first timing counter value (global time) to create a future timing counter value, wherein the offset amount includes the time to transfer a timing value from the first timing counter (313) of the first interface circuit (310) into a storage device (324) local to the second interface circuit (320) (col. 3, ll. 61-66; col. 4, l. 38 - col. 5, l. 61). Eatherton further discloses that the future timing counter value is created prior to copying said future timing value into the storage device that is local to the second interface circuit (col. 3, l. 66 - col. 4, l. 1; col. 4, ll. 21-23), thus reducing the number of steps carried out at the second interface circuit during the synchronization process.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Salee in view of Lovett to include adding the offset to the first timing counter value to create a future timing counter value and copying said future timing counter value into the storage device local to the second cable interface circuit, as taught by Eatherton, for the benefit of simplifying the synchronization process as carried out by the second cable interface circuit.

As to claims 12 and 21, the combination of Salee, Lovett, and Eatherton discloses the methods of claims 11 and 20 wherein said step of copying said future timing counter value from said storage device into said timing counter includes the steps of: (a) waiting a predetermined length of time (i.e., the predetermined update delay, Eatherton, col. 4, ll. 56-58) until said timing counter of the first cable interface circuit is substantially equal to said future timing counter value; and (b) copying said future timing counter value from

said storage device into said timing counter of the second cable interface circuit (Eatherton, col. 6, l. 60 - col. 7, l. 7).

As to claims 13 and 22, the combination of Salee, Lovett, and Eatherton discloses the methods of claims 11 and 20 wherein said step of copying said future timing counter value from said storage device into said timing counter includes the steps of: (c) waiting a predetermined length of time (i.e., the predetermined update delay, Eatherton, col. 4, ll. 56-58) until said timing counter of the first cable interface circuit increases to a value substantially equal to said future timing counter value; and (d) copying said future timing counter value from said storage device into said timing counter of the second cable interface circuit (Eatherton, col. 6, l. 60 - col. 7, l. 7).

As to claims 14 and 23, the combination of Salee, Lovett, and Eatherton discloses the methods of claims 11 and 20 wherein said step of copying said future timing counter value from said storage device into said timing counter includes the step of: (e) triggering the transfer of said future timing counter value from said storage device into said timing counter from a System Controller for said CMTS (Eatherton, col. 6, ll. 23-27).

As to claims 16-19 and 25-28, the combination Salee, Lovett, and Eatherton discloses the CMTS and synchronous clock systems of claims 15 and 24, but fail to explicitly disclose said system controller means is implemented as a microprocessor, an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), or sequential logic. Official notice is taken of the fact that it was well known in the art at the time of invention to implement a controller as: a microprocessor (which includes

sequential logic), thus enabling software-based control and reprogramming; an ASIC, thus enabling full hardware customization; and an FPGA, thus enabling reprogrammable hardware configurations. Accordingly, it would have been obvious to one of ordinary skill in the art to implement the system controller means of Salee, Lovett, and Eatherton as any of a microprocessor, an ASIC, an FPGA, and sequential logic, for the benefits discussed above.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

White et al., U.S. Patent Application Publication No. 2002/0038461, discloses synchronization of redundant CMTS line cards (¶ 61).

6. The following are suggested formats for either a Certificate of Mailing or Certificate of Transmission under 37 CFR 1.8(a). The certification may be included with all correspondence concerning this application or proceeding to establish a date of mailing or transmission under 37 CFR 1.8(a). Proper use of this procedure will result in such communication being considered as timely if the established date is within the required period for reply. The Certificate should be signed by the individual actually depositing or transmitting the correspondence or by an individual who, upon information and belief, expects the correspondence to be mailed or transmitted in the normal course of business by another no later than the date indicated.

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Please refer to 37 CFR 1.6(d) and 1.8(a)(2) for filing limitations concerning facsimile transmissions and mailing, respectively.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher M. Lambrecht whose telephone number is (571) 272-7297. The examiner can normally be reached on Mon-Fri, 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (571) 272-7353. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christopher M. Lambrecht
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Art Unit 2623

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